Power Device Package ~POL(Power Overlay)~

- Under development, sample is available -

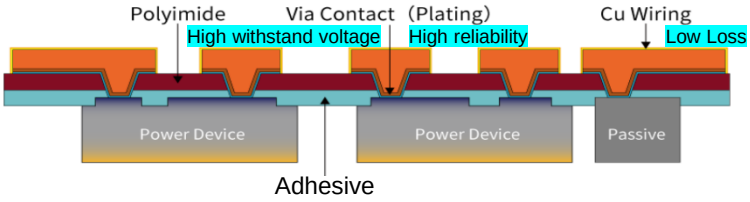
Features

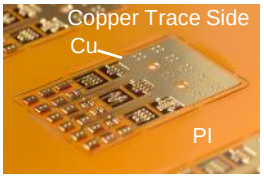
- Fully wire-bondless power semiconductor package solution
- High dimensional precision and stable shape reproducibility of circuit by photolithography
- Multiple chip package for high power density, low profile, low loss, high heat dissipation, high efficiency and reliability

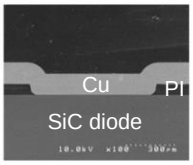
Structure

■ Standard

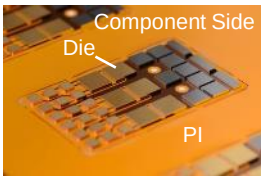
- Redistribution layer on isolation film above power device

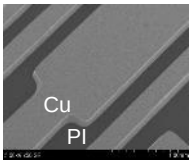






Φ750μm Via cross section



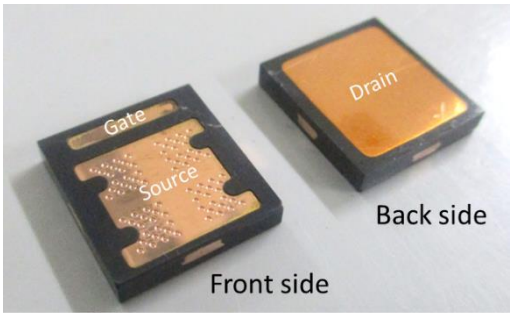


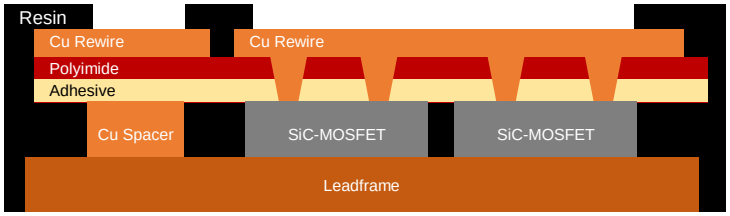
250μm Line/Space

■ Mold POL

- Construction of half-bridge or full-bridge circuits by attaching leadframe or DBC substrate on the bottom of chips
- Protect all components from the external environment by mold resin

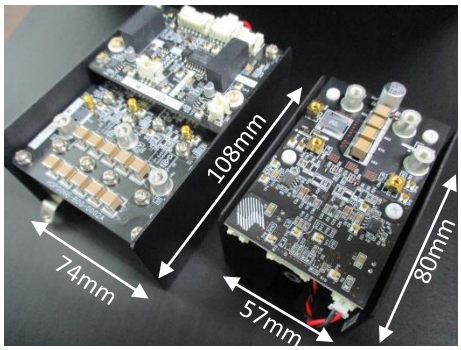
DBC : Direct Bonded Copper



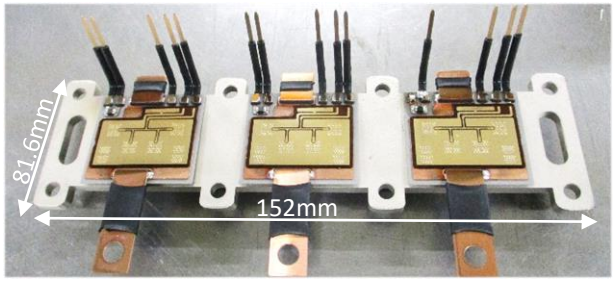


Examples

- Wide Band Gap semiconductors, e.g. GaN, SiC, embedded power supply units
- 40 to 50% volume down, GaN Half bridge block and SiC Full bridge block with POL



GaN Half Bridge Block



(SHINKO & Tohoku University Joint Research Theme)

SiC Full Bridge Block

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